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Post-CMOS Compatible Aluminum Scandium Nitride/2D Channel Ferroelectric Field-Effect-Transistor Memory

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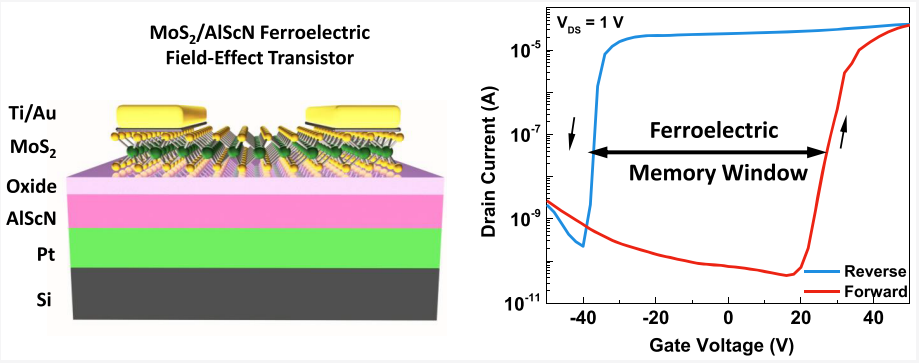

ABSTRACT: Recent advances in oxide ferroelectric (FE) materials have rejuvenated the field of low-power, nonvolatile memories and made FE memories a commercial reality. Despite these advances, progress on commercial FE-RAM based on lead zirconium titanate has stalled due to process challenges. The recent discovery of ferroelectricity in scandium-doped aluminum nitride (AlScN) presents new opportunities for direct memory integration with logic transistors due to the low temperature of AlScN deposition (approximately 350 °C), making it compatible with back end of the line integration on silicon logic. Here, we present a FE-FET device composed of an FE-AlScN dielectric layer integrated with a two-dimensional MoS_2 channel. Our devices show an ON/OFF ratio of ~10^6, concurrent with a normalized memory window of 0.3 V/nm. The devices also demonstrate stable memory states up to 10^4 cycles and state retention up to 10^5 s. Our results suggest that the FE-AlScN/2D combination is ideal for embedded memory and memory-based computing architectures.

KEYWORDS: *ferroelectric field effect transistor, memory, two-dimensional, MoS_2, CMOS, aluminum scandium nitride*

INTRODUCTION

In 1963, Moll and Tarui[1] suggested that the field-effect conductance of a semiconductor could be controlled by the remanent polarization of a ferroelectric (FE) material to create a ferroelectric field-effect transistor (FE-FET). However, subsequent efforts to produce a practical, compact FE-FET have been plagued by low retention and incompatibility with complementary metal oxide semiconductor (CMOS) process integration. These difficulties led to the development of trapped-charge-based nonvolatile memory (NVM) devices (a.k.a. floating gate or flash memory).[2] The emergence of perovskite oxides with stable and tunable FE properties has rejuvenated the fields of electroceramics and solid-state devices that rely on strong intrinsic polarization. These perovskite oxides have now made FE random access memories (FE-RAM) a commercially viable product.[3−5] However, the ferroelectricity in perovskite oxides, while stable, is highly suceptible to strain and oxygen content (stoichiometry). Therefore, it is difficult for oxide FE materials to survive harsh micro- and nanofabrication processes or high temperatures.[6] Only recently has ferroelectric hafnium−zirconium oxide been deposited at CMOS BEOL compatible temperatures. However, low-T deposition results in the dielectric lacking the desirable breakdown strength.[7,8] In this regard, more chemically, electrostatically, and thermally stable FE dielectrics are desired, particularly for back end of the line (BEOL) processes.[9]

Further, there is a critical need and demand for memory devices that can be closely coupled to logic transistors. The slowdown in Moore's Law[10] and the emergence of the memory bottleneck in utilizing Big-Data[11] has created an urgent need

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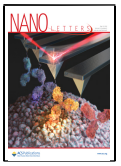

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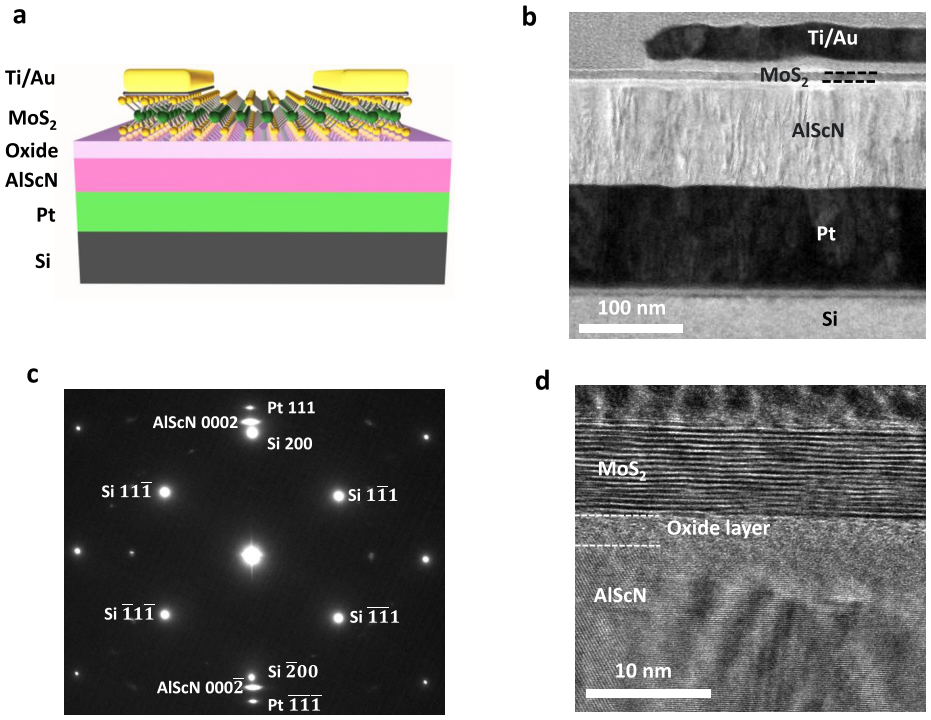

Figure 1. Multilayer MoS_2FE-FETs with a 100 nm thick AlScN ferroeletric. (a) Schematic view of a AlScN/MoS_2 FE-FET. The gate stack includes 100 nm Pt on Si as the gate electrode and 100 nm AlScN as the ferroelectric gate dielectric. An ∼3 nm native oxide layer naturally occurs on top of ferroelectric AlScN due to ambient air exposure. (b) Cross-sectional TEM image of a representative sample showing the source-drain contact, MoS_2 channel, amorphous oxide, and polycrystalline AlScN gate dielectric. (c) SAED pattern of a ferroelectric AlScN film showing templating along [0001] (*c* plane). (d) High-resolution phase-contrast TEM image obtained from the channel/dielectric interface in (c) where the individual MoS_2 layers in the channel and surface oxide layer are visible.

for low-power, highly scalable memory devices. These needs require the development of computing hardware architectures different from the standard von Neumann architecture and require tight integration with on-chip memory devices.[12,13] New applications such as the Internet of Things (IoT) and artificial intelligence (AI) algorithms—applications that either generate or consume vast amounts of data[14,15]—create a strong demand for high-density NVM. FE-NVM devices are the most compelling due to their simple device structure, higher access speed, high endurance, and extremely low write energy.[16−20] Although ferroelectric random-access memory (FE-RAM) is an extant commercial technology, the device architecture requires an FE capacitor to be connected in series with a transistor. Further, the readout of a FE-RAM cell overwrites the FE capacitor by switching its polarity to extract the read current signal. The FE-FET overcomes the above challenges. However, several persistent challenges have prevented the creation of scalable and durable FE-FETs:

(1) the lack of a ferroelectric material with sufficiently large coercive field and remnant polarization[17−20]
(2) the incompatibility of viable ferroelectric dielectrics with standard CMOS processing[19]
(3) poor retention due to large depolarization fields[20]

Here, we demonstrate a high-performance FE-FET that integrates an atomically thin, two-dimensional (2D) molybdenum disulfide (MoS_2) channel on top of an AlScN dielectric. The devices achieve an ON/OFF ratio of ∼10^6 between the two memory states of "0" and "1". The AlScN dielectric is deposited onto a Si substrate at temperatures below 350 °C, making the process compatible with BEOL CMOS integration. We build upon recent reports showing that the remnant polarization (P_r) of AlScN can be very high (80−115 $\mu C/cm^2$) when Sc concentrations exceed 27%.[9] The key advantage of the high remnant polarization is that the instabilities induced by both charge trapping and leakage currents through the ferroelectric insulator do not significantly affect the FE-FET device performance. Also, the higher coercive fields exhibited by AlScN (2−4.5 MV/cm) are effectively immune to the depolarization fields for a given polarization, which helps achieve long retention times and reduce read-disturb. While a larger E_c value also means a larger write field, this should not be an issue as long as the ferroelectric thickness can be scaled down without inducing significant leakage. To this end we have made some progress with thinner FE-AlScN films in recently published works.[21] Ultimately, a large coercive field is very important and necessary to prevent against random bit-flip errors and read-disturb. This issue is particularly well-known for the case of PZT ferroelectrics.[22,23] In addition, we also note that van der Waals 2D semiconductors such as MoS_2 can be transferred onto arbitrary substrates at room temperatures via wet- or dry-transfer schemes.[24,25]

It is also worth noting that although FE-FETs from 2D channels such as MoS_2 have been demonstrated and AlScN is a known ferroelectric dielectric, there have been no FE-FET demonstrations using AlScN, in part because the growth of columnar, well-oriented FE-AlScN does not occur on Si or other mature semiconductors. Therefore, to evaluate AlScN's performance in an FE-FET, one needs to transfer or deposit a high-quality semiconductor on as-grown FE-AlScN and 2D semiconductors such as MoS_2 are ideal in this regard. Further, the P_r value of FE-AlScN is quite high in comparison to other known FE dielectrics. The effect of such a high P_r on any

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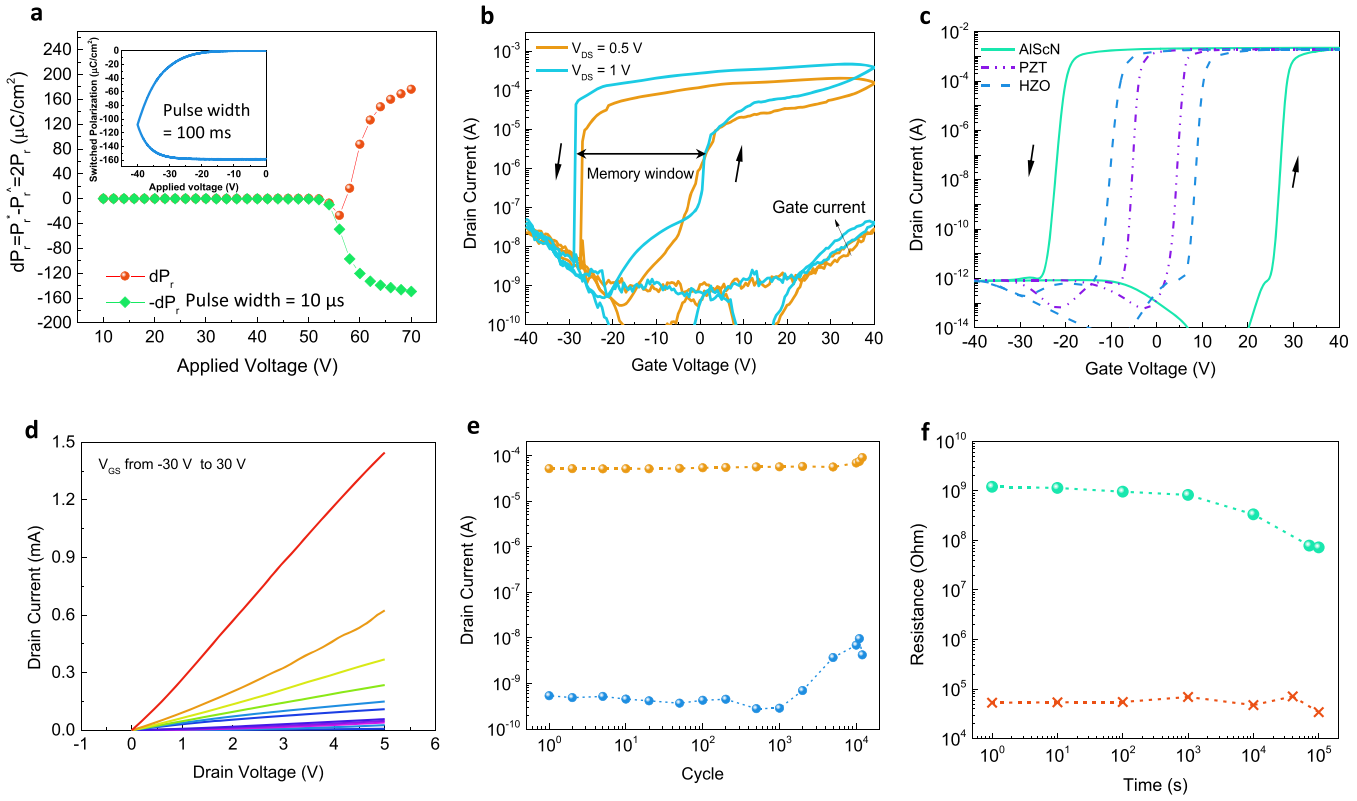

Figure 2. Room-temperature electrical characterization of AlScN/MoS_2FE-FETs. (a) PUND results of a 100 nm AlScN thin film with a pulse width of 10 μs and 1 ms delay between pulses. The PUND test reveals a saturated remanent polarization of 80 $\mu C/cm^2$ and a ferroelectric switching voltage over 50 V. The inset is a monopolar triangular wave PUND with 100 ms pulse width and a zero to peak voltage of 40 V, suggesting a ferroelectric switching voltage between 30 and 40 V. (b) Semilogarithmic scale transfer characteristics at room temperature of a representative AlScN/MoS_2 FE-FET with 100 nm AlScN as the ferroelectric gate dielectric. The channel length is 3.2 μm, and the channel width is 14.8 um for the device shown. The arrows show the clockwise hysteresis of the drain current, which is consistent with the accumulation and depletion of electrons. The device exhibits a large memory window (~30 V) (counterclockwise hysteresis loop) and on/off drain-to-source resistance ratio of up to 10^6. (c) TCAD simulations of MoS_2 FE-FETs with ferroelectric dielectrics of 100 nm thick PZT, HfO_2, and AlScN, respectively, showing counterclockwise transfer curve hysteresis loops. (d) Linear-scale output characteristics of the same device at various gate voltages. (e) Endurance measurements of the ON and OFF memory states of the FE-FETs with the number of gate voltage cycles. The gate voltage cycle ranges were from −40 to +40 V. (f) Resistance state retention measurement obtained by programming the ON or OFF state with a gate voltage of ±40 V and then monitoring the drain current for varying time intervals up to 100000 s.

semiconducting channel is untested, and therefore using 2D semiconducting channels that present the ultimate limit in carrier density modulation and inducing a depolarization field is something that our work accomplishes and adds constructively to the body of knowledge on both 2D FETs and FE-FETs. Finally, the 2D channel combined with large P_r ferroelectric presents an ideal scenario for long retention in FE-FETs, which is a longstanding goal for this device technology, and our work aims to take a stepping stone in that direction. The above arguments in combination with the CMOS compatibility of AlScN suggest that our approach could lead to a new generation of scalable, high-performance, and low-power memory devices compatible with Si CMOS processors.

■ STRUCTURE OF MoS_2 FE-FETS WITH FERROELECTRIC AlScN

The AlScN/MoS_2 FE-FETs are bottom-gated transistors with 100 nm thick $Al_{0.71}Sc_{0.29}N$ grown by sputter deposition on a 100 nm thick Pt template (Figure 1a) that was deposited on a heavily doped Si (100) wafer (see methods in the Supporting Information for details). A cross-sectional bright-field transmission electron microscopy (TEM) image of a representative AlScN/MoS_2 FE-FET is shown in Figure 1b (see Figure S3 in the Supporting Information for elemental analysis). The corresponding selected area electron diffraction (SAED) image pattern shows that the ferroelectric AlScN is highly crystalline and textured along the [0001] growth direction, evident in the arc of the 0002 reflection (Figure 1c). A high-resolution phase-contrast TEM image of the AlScN/MoS_2 interface is shown in Figure 1d, and the few-layer MoS_2 channel layer is clearly visible. A thin oxide layer is also observed on the top surface of AlScN. The thin (<5 nm) layer does not play a critical role in the switching of the FE-AlScN[26] in the demonstrated FE-FETs. A detailed description and discussion of the role of oxide are presented in section S11 in the Supporting Information.

■ PERFORMANCE OF AlScN/MoS_2 FE-FETS

The ferroelectric response of the 100 nm AlScN thin film was characterized by a positive-up, negative-down (PUND) measurement using a 10 μs square wave with a 1 ms delay between the two pulses (Figure S4a in the Supporting Information), as shown in Figure 2a. The PUND test was preferred over a polarization−electric field hysteresis loop (P-E loop) because the P-E loop of 100 nm AlScN shows a polarization-dependent leakage that hinders the observation of

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polarization saturation on the positive field side (Figure S4c in the Supporting Information).[27] The PUND result indicates a remanent polarization of ~80 μC/cm^2 in the AlScN film, and the onset of ferroelectric switching is over 50 V for a 10 μs pulse. Since the coercive voltage of a ferroelectric thin film can be associated with the frequency (or pulse width) of the applied voltage,[9,28−31] another PUND test using a monopolar triangular wave with a 100 ms pulse width and a zero to peak voltage of 40 V was conducted and is presented as the inset of Figure 2a (see also Figure S4b in the Supporting Information). This PUND measurement indicates the same remanent polarization of ~80 μC/cm^2 and a switching voltage between 30 and 40 V under conditions similar to those of the device measurement and simulations. The formation of a native oxide on the surface of the FE-AlScN also gives an opporunity to fabricate MIM capacitor devices with the FE layer forming a leaky dielctric, while the thin-film oxide is an insulating tunnel barrier layer. A nonvolatile resistive switching in the form of a ferroelectric tunnel junction at an applied DC voltage of 30−40 V was also observed, which serves as complementary evidence in support of ferrolectric switching (Figure S5 in the Supporting Information).

In addition to standard current−voltage measurements, hysteresis between transfer characteristics was measured for the FE-FETs along two different sweep directions: (i) forward (from low to high current, i.e. negative to positive gate voltage) and (ii) reverse (from high to low current and positive to negative gate voltage) gate voltage sweeps at two different drain voltages (Figure 2b). The application of a positive gate bias results in a sharp increase in drain current by several orders of magnitude associated with strong electron accumulation and a remanent on-state current after the bias is brought back to the read voltage window. The transistor shows an an n-type characteristic due to the n-doping induced by the presence of sulfur vacancies in MoS_2.[32] Upon a switch from positive bias to negative gate bias, a gentle decrease in current followed by a precipitous drop at ~−30 V is observed. This suggests channel depletion and a remanent off-state current. The drain current after depletion is reached (off-state) closely mimics the gate current, which indicates that it is due to leakage from the gate insulator. The measured ON/OFF current ratios of the reported devices are ~10^6. We speculate that the source of this leakage current is likely due to the large areas of contact pads and global back gate combined with imperfections in the AlScN film or underlying Pt, which can be minimized by using a local gate geometry or using an additional insulating layer underneath the probe contact pads in our devices.

The hysteresis in the reported transfer curves is significant and counterclockwise in its directionality, consistent with FE-FET theory.[33−36] Charge trapping in dielectrics is also known to produce hysteresis loops in transfer curves. However, trapping-induced hysteresis loops are only clockwise in their directionality. Hence, our observation of a counterclockwise ferroelectric loop suggests the existence of ferroelectricity and polarization switching. With 100 nm thick AlScN as a ferroelectric dielectric, the resulting AlScN/MoS_2 FE-FETs exhibit a large memory window of ~35 V. The normalized memory window at a drain voltage of 1 V, divided by the thickness of the ferroelectric film, is 0.3 V/nm. This large normalized memory window is attributed to the desirable ferroelectric properties of AlScN: large coercive field, high polarization, and moderate dielectric constant. We also performed technology computer-aided design (TCAD) simulations to investigate the dependence of the memory window on the ferroelectricity of the gate dielelctric, by adopting the FE parameters of traditional lead zirconium titanate (PZT), doped hafnium oxide (HfO_2), and AlScN (Table S1 in the Supporting Information). As shown in the simulation results in Figure 2c, counterclockwise transfer curve hysteresis loops are observed in all three FE-FETs with MoS_2 channels and with 100 nm thick gate dielectrics with the largest memory window for AlScN. We note that the memory windows in simulated I_D-V_G curves in Figure 2c are symmetrical at about V_G = 0 V while the experimentally measured transfer characteristics of the device have been shifted left in comparison. We attribute this to traps at the interface of the semiconductor and in the AlScN dielectric as well as the surface oxide (see section S10 in the Supporting Information for details).

To further characterize the channel properties, the output characteristics (drain current−drain voltage) of AlScN/MoS_2 FE-FETs were measured. They show a linear behavior with a large degree of current control (current ratio of 10^4) up to a high drain bias of 5 V and a large drive current density of over 100 μA/μm in the ON State. This ON current density is comparable with some of the highest current density values reported using electrical double-layer dielectrics[37] or ultrathin atomic layer deposition grown dielectrics.[38] A maximum drain current over 1.4 mA is achieved with the 100 nm thick AlScN ferroelectric, and the channel length is 3.2 μm. To further determine the memory effect and reliability, we performed cycling and time varying retention tests between the ON/OFF states as shown in Figure 2e,f. Figure 2e presents remanent ON-state and OFF-state currents extracted from 12000 cycles. Cyclic program/erase operations of the same AlScN/MoS_2 FE-FET indicate that the both ON and OFF current states are stable and rewritable and do not show appreciable degradation up to 10000 cycles. Readouts at various delay times were carried out to determine retention (Figure 2f). The low and high current/resistance states can be retained for at least 100000 s at room temperature without significant degradation. We emphasize that a 2D channel is critical in achieving not only a high ON/OFF ratio but also long retention due to a minimal depolarization field.[20] The switching speed in the reported FE-FETs with 100 nm AlScN should be comparable to the switching speed of <200 ns in 45 nm thick AlScN MIM capacitors, as demonstrated in our recent study, which also shows cycle endurance similar to that observed in the FE-FETs presented here.[26] A FE-FET is different in comparison to an MIM capacitor and has additional parasitic elements in terms of contact and channel resistances. However, at our dielectric thicknesses (100 nm) and channel dimensions (>1 um) these factors are unlikely to be limiting the switching speed.

■ COMPARISON OF AlScN/MoS_2 FE-FETS WITH REFERENCE AlN/MoS_2 FETS

To further reinforce our observations from electrical measurements, we fabricated reference AlN/MoS_2 FETs. An AlN film of thickness identical with that of AlScN was sputtered in the same system under the same conditions. Then AlN/MoS_2 FETs with similar channel thicknesses and channel dimensions were fabricated using the same process flow used for the AlScN/MoS_2 FE-FETs. Transfer curves on both AlScN/MoS_2 FE-FETs and AlN/MoS_2 FETs with various sweep ranges are shown in Figure 3. The hysteresis loops in the transfer

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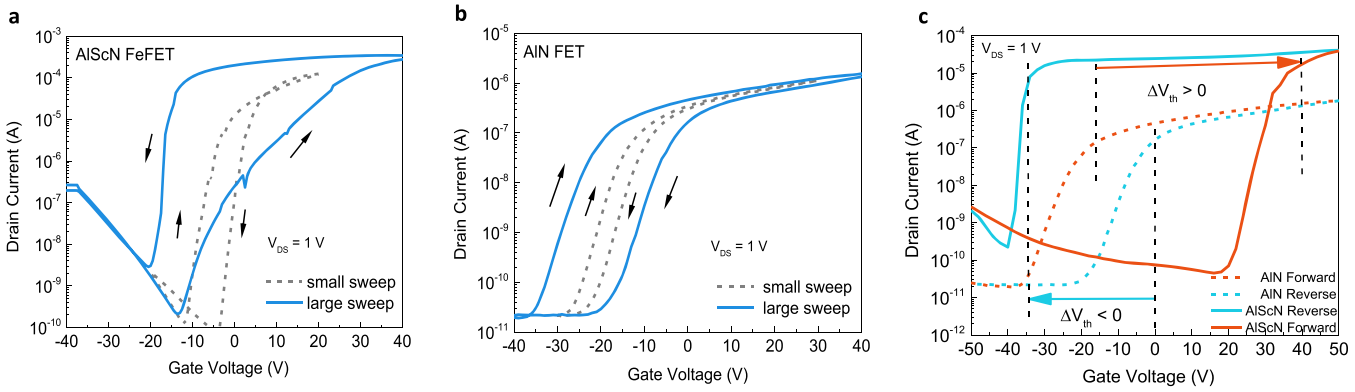

Figure 3. Comparison of AlScN/MoS_2FE-FETs with reference AlN/MoS_2FETs. (a) Semilogarithmic scale transfer characteristics at room temperature of a representative AlScN/MoS_2 FE-FET with a large gate voltage sweep range (solid blue line) and a small gate voltage sweep range (dashed gray line). The device has an AlScN thickness of 100 nm, a channel length of 3.75 μm, and a channel width of 15 μm. The arrows show the hysteresis directionality of the transfer curves. For a small sweep range (from −20 to +20 V), the hysteresis is observed to be clockwise, indicating charge trapping and no ferroelectric switching. Conversely, for a large sweep range, the hysteresis is observed to be counterclockwise, indicating the occurrence of FE polarization switching. (b) Semilogarithmic scale transfer characteristics at room temperature of a representative AlN/MoS_2 FET with both a large gate sweep range (solid blue line) and a small gate sweep range (dashed gray line). The device has an AlN gate thickness of 100 nm, a channel length of 3.6 μm, and a channel width of 10 μm. For both small and large gate voltage sweep ranges, the hysteresis is observed to be clockwise, indicating that charge traps dominate the threshold voltage shifts and that no ferroelectricity is present. (c) Comparative transfer characteristics during both forward and back ward sweeps in the ±50 V range for AlScN and AlN dielectric MoS_2 FETs. The clear and opposite signs of threshold voltage shifts between the AlScN/MoS_2 FE-FET and Athe lN/MoS_2 FET for forward (red) and reverse (blue) sweeps are shown. The large differences in ON currents between the two transistors and the marked enhancement in steepness of the subthreshold swing in AlScN-based MoS_2 FETs in comparison to AlN-based FETs are also evident.

characteristic, which depend strongly on the gate voltage sweep range, serve as strong evidence of ferroelectric polarization switching in AlScN/MoS_2 FE-FETs for DC measurements. As shown in Figure 3a, the hysteresis in the AlScN/MoS_2 FE-FET transfer curve is observed to reverse from clockwise to counterclockwise with the onset of polarization switching, which occurs at a higher gate voltage. For a small sweep range, the hysteresis is observed to be clockwise, indicating that charge trapping is dominating the observed current hysteresis and that the ferroelectric polarization has not been reversed. For a large sweep range, the hysteresis is observed to be counterclockwise, indicating the onset of polarization switching of the ferroelectric. As shown Figure 3b, MoS_2 FETs on 100 nm AlN show regular n-type behavior with an ON/OFF value of ∼10^5 similar to those made on oxide dielectrics. Significant hysteresis has also been observed, comparable to that of oxide dielectrics, but in the clockwise direction only. We attribute this to the trapped charge in the defects and dangling bonds in the dielectrics. Moreover, the hysteresis loop direction for the AlN dielectric FETs does not flip sign upon an extension of the sweep range up to ±70 V (Figure S6 in the Supporting Information). This further suggests that the counterclockwise hysteresis in AlScN/MoS_2 FE-FETs is induced by ferroelectric polarization switching.

Another striking observation is the difference in the magnitudes of the ON currents between the AlN/MoS_2 FETs and the AlScN/MoS_2 FE-FETs for similar channel dimensions, thicknesses, dielectric constants, and dielectric thicknesses (Figure 3c). Given that the k value of AlScN (∼12) is only ∼1.7× greater than that of AlN (∼7.1), a difference in ON current density by 400× is inexplicable by the standard dielectric capacitive charging model. This again suggests the presence of a high surface charge density in the semiconductor channel, which is induced by the ferroelectric polarization of AlScN. In addition to the current magnitude, the comparative shift in threshold voltages of the transfer characteristics between AlN/MoS_2 FETs and AlScN/MoS_2 FE-FETs upon forward and reverse sweeps also suggests the presence of ferroelectric polarization in AlScN (Figure 3c). For the forward sweeps (red), the shift in threshold voltage between AlScN/MoS_2 FE-FETs and AlN/MoS_2 FETs is positive, indicating an additional negative charge at AlScN/MoS_2 interface. In contrast, for the reverse sweeps (blue), the shift in threshold voltage between AlScN/MoS_2 FE-FETs and AlN/MoS_2 FETs is negative, indicating an additional positive charge at the AlScN/MoS_2 interface. This change in sign of the charge at the AlScN/MoS_2 interface further verfies that the significant hysteresis induced in the transfer characteristics is a result of ferroelectric polarization switching. Finally, the dissimilarity of the subthreshold swing slope (SS) between AlN/MoS_2 FETs and AlScN/MoS_2 FE-FETs also indicates that the density of carriers in the channel is dominated by ferroelectric polarization switching. As shown in Figure 3c, the demonstrated MoS_2 FETs on AlScN exhibit steep slope-switching behavior (100 mV/dec) in comparison to the MoS_2 FETs on AlN of the same thickness (3000 mV/dec), reducing the subthreshold swing by 2 orders of magnitude. The abrupt and dramatic switching behavior displayed in Figure 3c is a direct effect of negative capacitance by integrating a ferroelectric layer into the gate.[39−41] As a consequence of negative capacitance, the FET device can operate with an SS value of less than 60 mV/dec at room temperature in addition to exhibition of negative drain-induced barrier lowering (Figures S7 and S8 in the Supporting Information), which further verifies our claim of FE switching.

BENCHMARKING AND DISCUSSION

The above results show that FE-AlScN and 2D MoS_2 channel-based FE-FETs are appealing. However, a thorough benchmarking with FE-FETs in the literature is desired to enable a fair assessment and technological viability. FE-FETs using 2D semiconductors are well-known and have been fabricated/demonstrated in the past.[42−46] However, AlScN-based FE-

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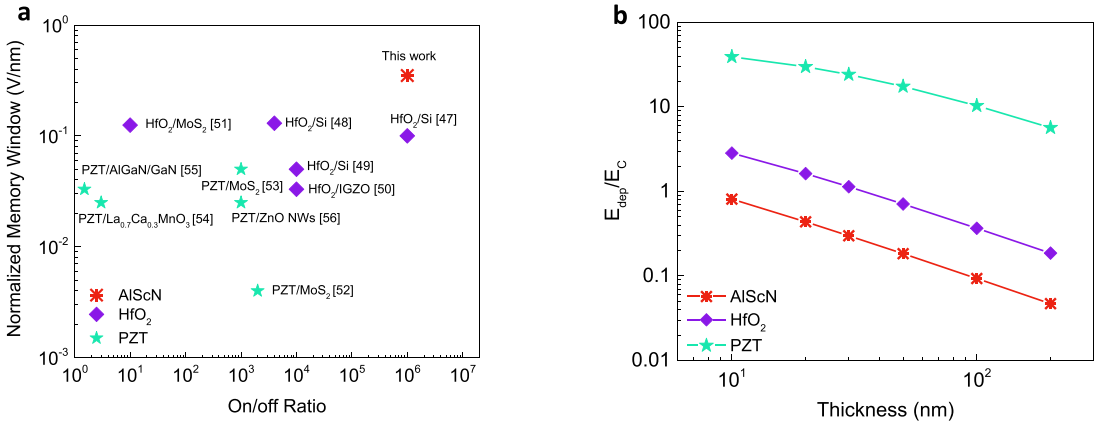

Figure 4. Performance comparison of the AlScN/MoS_2FE-FETs with previously reported FE-FETs, including tradional PZT FE-FETs and the state of the art HfO_2FE-FETs. (a) ON/OFF current ratios and normalized memory window from the reported Fe-FETs in the literature with HZO and PZT dielectrics paired with Si and 2D semiconductor channels.[47−56] It is worth noting that the reported AlScN-based FE-FET lies closest to the top-right corner of the plot. (b) Calculated ratio of depolarization field over coercive field (E_{dep}/E_c) in three different FE-FET cases: (1) AlScN + 1 nm buffer layer; (2) HfO_2 + 1 nm buffer layer; (3) PZT + 1 nm interfacial insulating layer shown as a function of varying thickness of the FE dielectric. The E_{dep}/E_c ratio in AlScN FE-FETs is much smaller than those of its HfO_2 and PZT FE-FET counterparts with an E_{dep}/E_c ratio of less than 1 even when the ratios are scaled to 10 nm thicknesses.

FETs have yet to be made. Combining a 2D channel with a BEOL-compatible ferroelectric that has high remnant polarization is an interesting and unique combination for ultimately obtaining a long retention time, which remains a holy grail for FE-FETs as a technology. Our work represents an important stepping stone in this direction. Figure 4a shows a comparison of AlScN/MoS_2 FE-FETs with previously reported FE-FETs including traditional PZT FE-FETs and the state of the art HfO_2-based FE-FETs.[47−56] Si channels, 2D MoS_2 channels, etc. have been used for the comparison. We have extracted the ON/OFF current ratio and a normalized memory window (memory window/ferroelectric thickness) from the reported transfer curves for a fair benchmarking. Normalization of the memory window to FE thickness is essential for the comparison, since all FE materials used and reported in the literature have varying thicknesses and because the memory window is propotional to the product of ferroelectric thickness and coercive field. Figure 4a clearly indicates that AlScN/MoS_2 FE-FETs outperform all previous FE-FETs in terms of normailized memory window and, more importantly, AlScN/MoS_2 FE-FETs fullfill the two metrics (sufficient memory window and high ON/OFF current ratio) concurrently (see additional discussion in section S15 in the Supporting Information). Further, near room-temperature transfer of wafer-scale CVD-grown 2D semiconductors has also been achieved.[58] Therefore, the device concept presented has the highest potential to be scaled up and ultilzed in CMOS BEOL applications among all the demonstrated FE-FETs.

While our reported FE-FETs are superior in terms of ON/OFF ratio and memory window, the endurance and retention are equally critical for a memory. One drawback that the FE-FET device concept has traditionally encountered is the depolarization of the ferroelectric layer over time due to the electrical field induced by incomplete charge compensation of the semiconducting channel.[57] To investigate the depolarization field in the proposed AlScN FE-FET and its counterparts (PZT and HfO_2 FE-FET), we calculate the depolarization field/coercive field (E_{dep}/E_c) ratio in the FE-FETs. As shown in Figure 4b, even for a scaled 10 nm AlScN ferroelectric layer, we derive an E_{dep}/E_c ratio less than 1, indicating that the depolarization field does not exceed the coercive field for the ferroelectric layer. In contrast, both HfO_2- and PZT-based FE-FETs have E_{dep}/E_c ratio of ∼3 and ∼40, respectively. This suggests that low-voltage scaling of AlScN/2D channel-based FE-FETs concurrent with long retention is attainable (see sections S12 and S15 in the Supporting Information for additional discussions). Further, ferroelectricity in <10 nm AlScN has already been demonstrated[59] and the lateral scaling advantages for 2D channels are already well-proven.[60] In the intermediate to long term, the most important challenge would be to limit leakage in <10 nm FE-AlScN films. This is an active area of research in the community and also a basis of our ongoing future efforts, which are beyond the scope of this current work on an FE-FET demonstration using AlScN with 2D semiconductor channels.

In summary, we have shown high-performance FE-FET based memory devices using an AlScN FE dielectric combined with a 2D MoS_2 channel that exhibit a record normalized memory window and ON/OFF ratio concurrently with good retention and CMOS BEOL compatible processing temperatures.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.0c05051.

Optical and electron micrographs of devices and additional electrical characterizations and simulations (PDF)

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Author Contributions

D.J., R.H.O., E.A.S., and X.L. conceived the idea. X.L. designed memory devices and performed electrical measurements. X.L. and K.K. performed all simulations and modeling. X.L., K-H.K., and J.M. performed microfabrication. D.W. performed P-E loop and PUND measurements. J.Z. performed ferroelectric material growth. P.M. performed transmission electron microscopy characterization. D.J., R.H.O., E.A.S., and X.L. analyzed and interpreted the data. D.J., R.H.O., and E.A.S. supervised the study. All others contributed to writing the manuscript.

Notes

The authors declare the following competing financial interest(s): D.J., X.L., R.H.O., and E.A.S. have a provisional patent filed based on this work. The authors declare no other competing interests.

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